**Report on Analog Assignment**

**Analog And Digital VLSI Design EEE F313/INSTR F313**



**Birla Institute Of Technology And Science, Pilani**

**TOPIC: Design a Single-ended output Folded Cascode [Differential amplifier + common gate stage] OPAMP**

**Submitted By:**

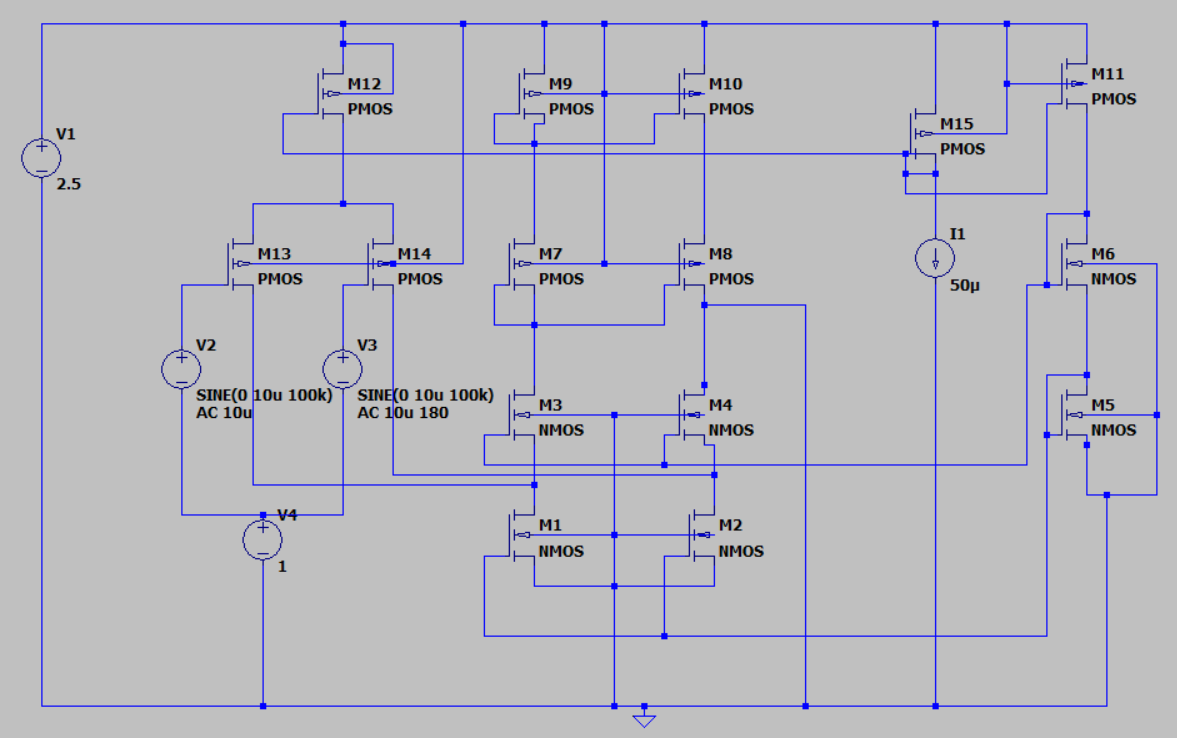
Vaidik A Sharma 2021B5A82509P Deeksha Agarwal 2022A3PS0500P

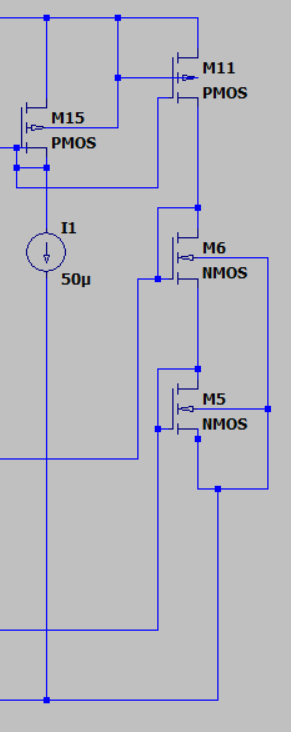
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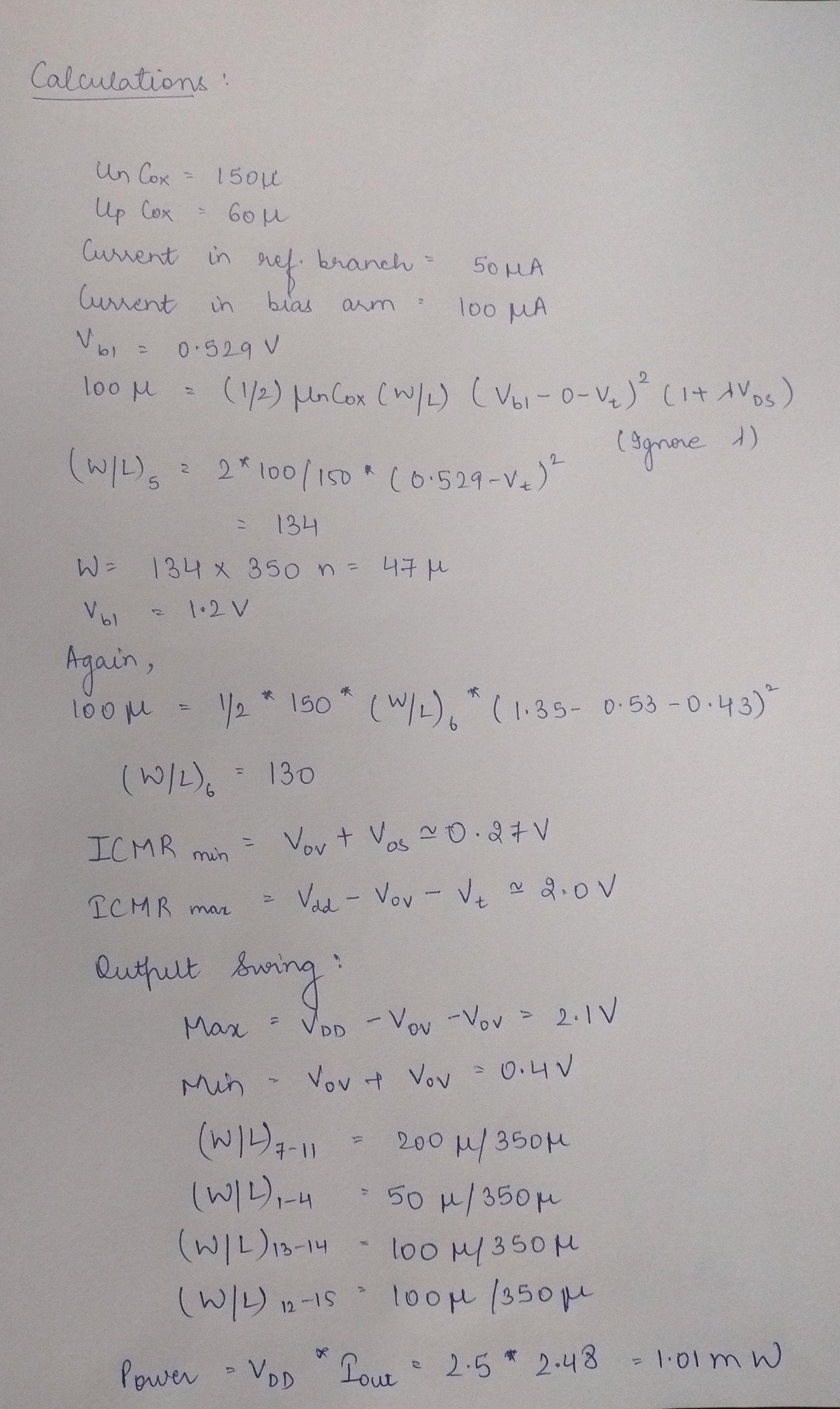
**PROBLEM STATEMENT:** *Design a Single-ended output Folded Cascode [Differential amplifier + common gate stage] OPAMP. Use PMOS as the input transistor.*

1. Analog schematic for OTA
2. Analysis of all equations for OTA, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications.
   1. ICMR ≥ 1.8 V
   2. CMRR ≥120dB
   3. output Swing ≥ 2V
3. Show a biasing circuitry to bias all the voltages in your design (except the input).
4. Use STB analysis to measure the closed loop gain and phase margin.
5. Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, CMRR plot, ICMR plot, PSRR plot, slew rate, Output voltage swing (dc + Transient), power consumption, and input and output offset voltage.

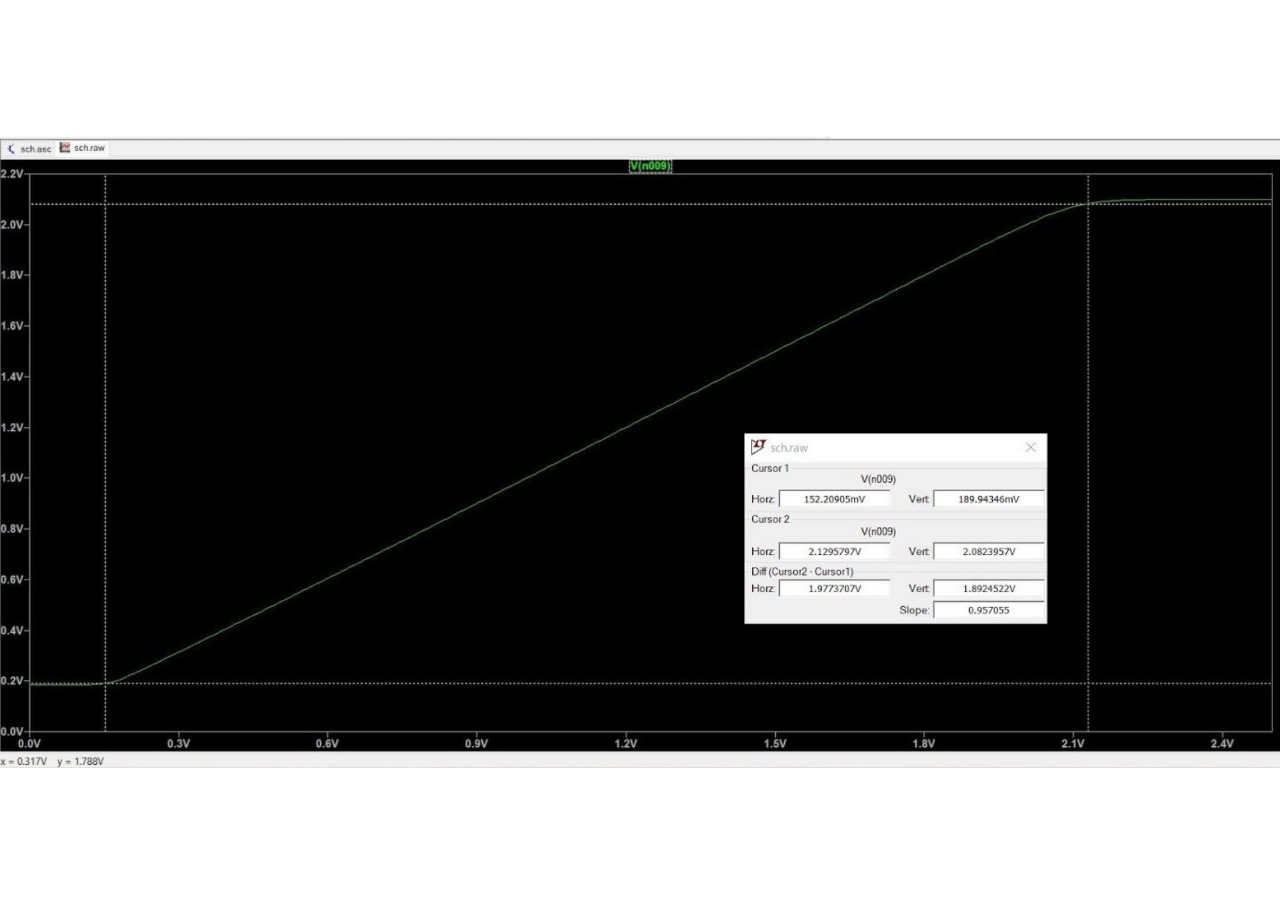
**Circuit Schematic:**

**Biasing Part of Circuit:**

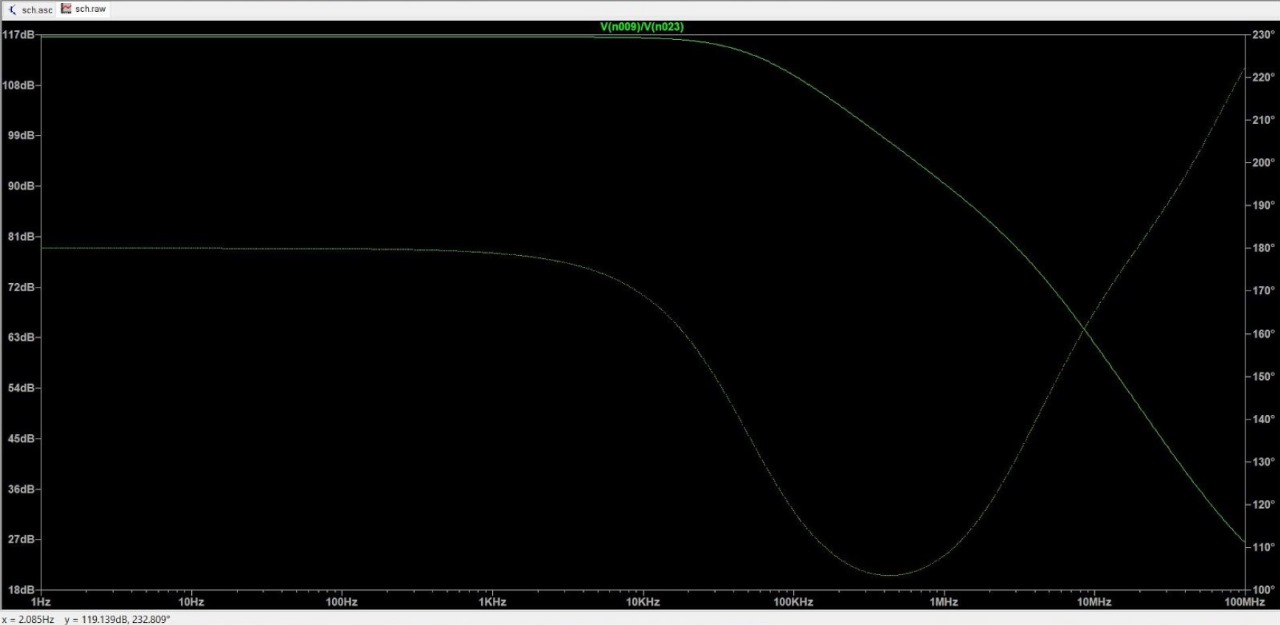
**Calculations -**



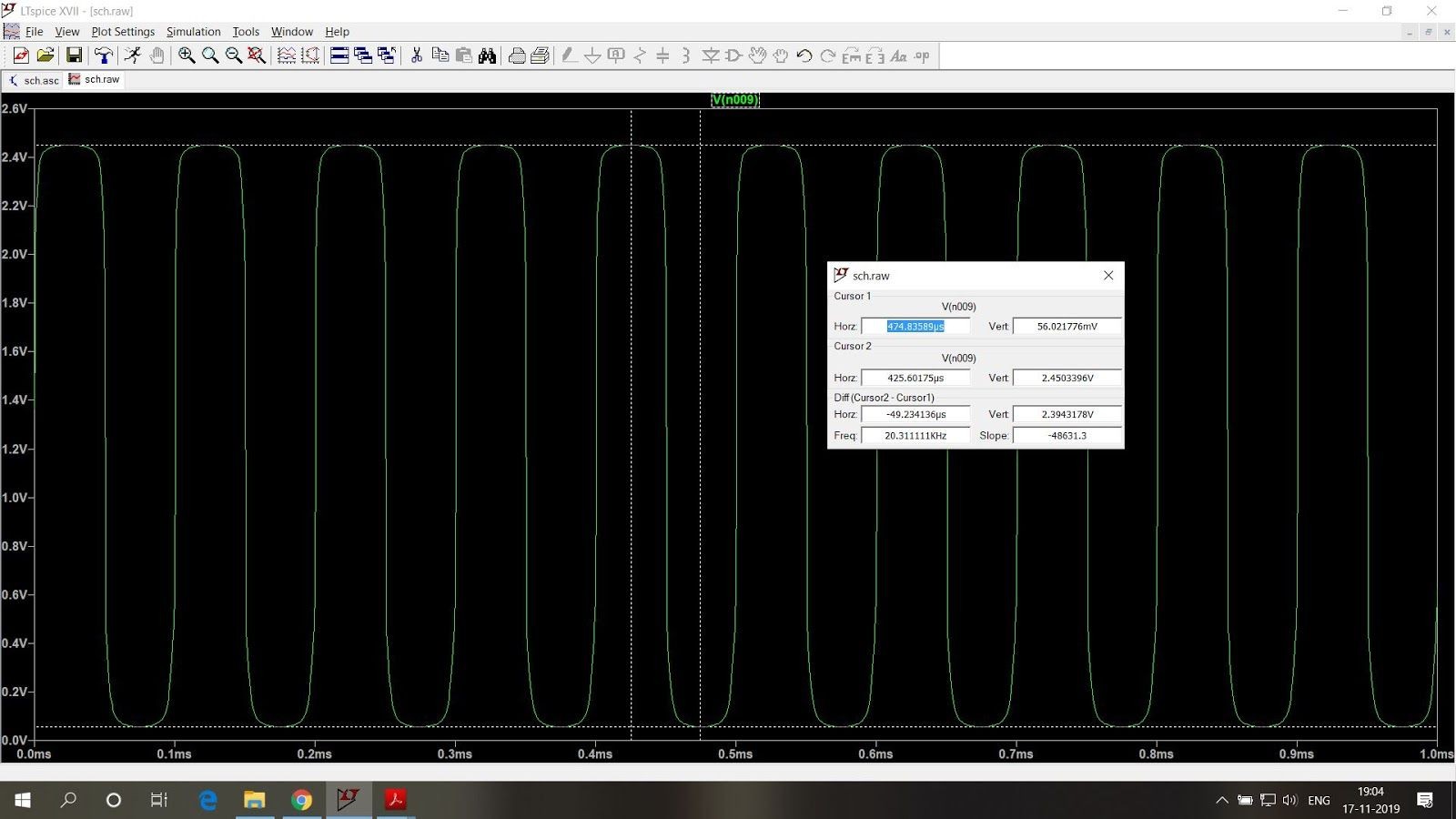
**Condition Simulations and Plots –**

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*Fig 1. ICMR = 1.97v > 1.8v*

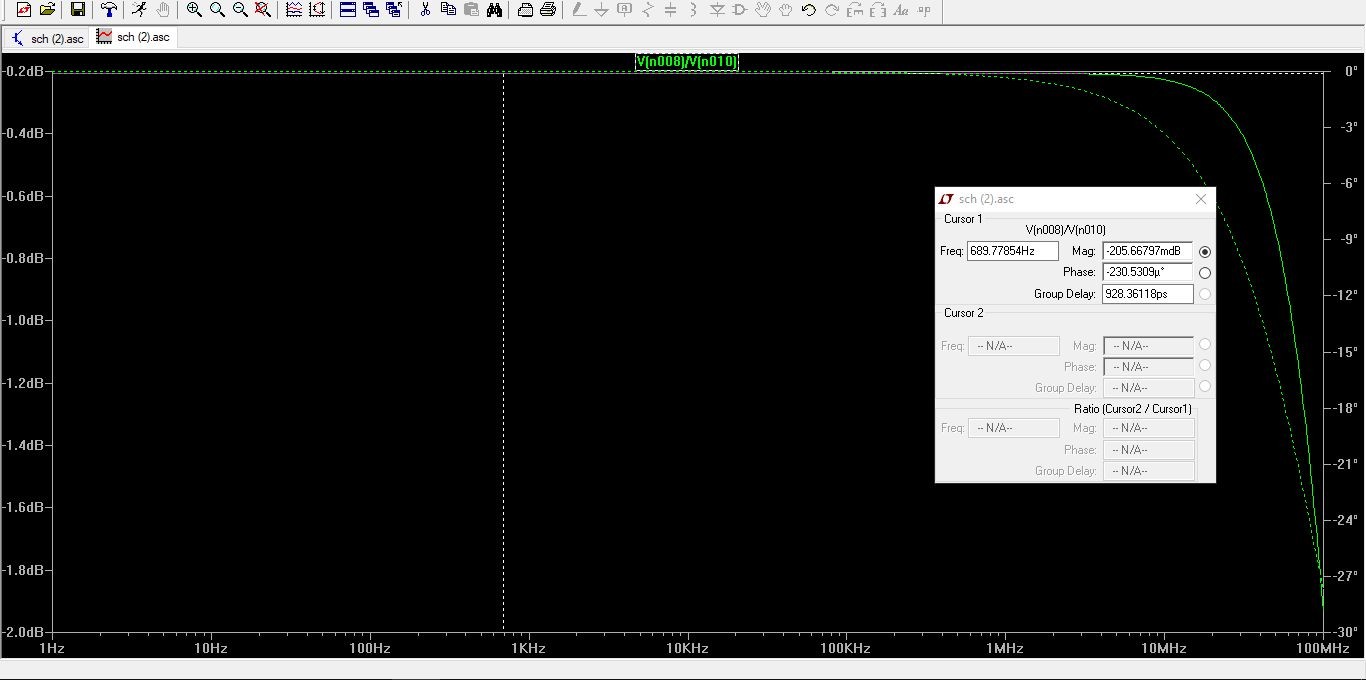


*Fig 2. CMRR = 117dB*

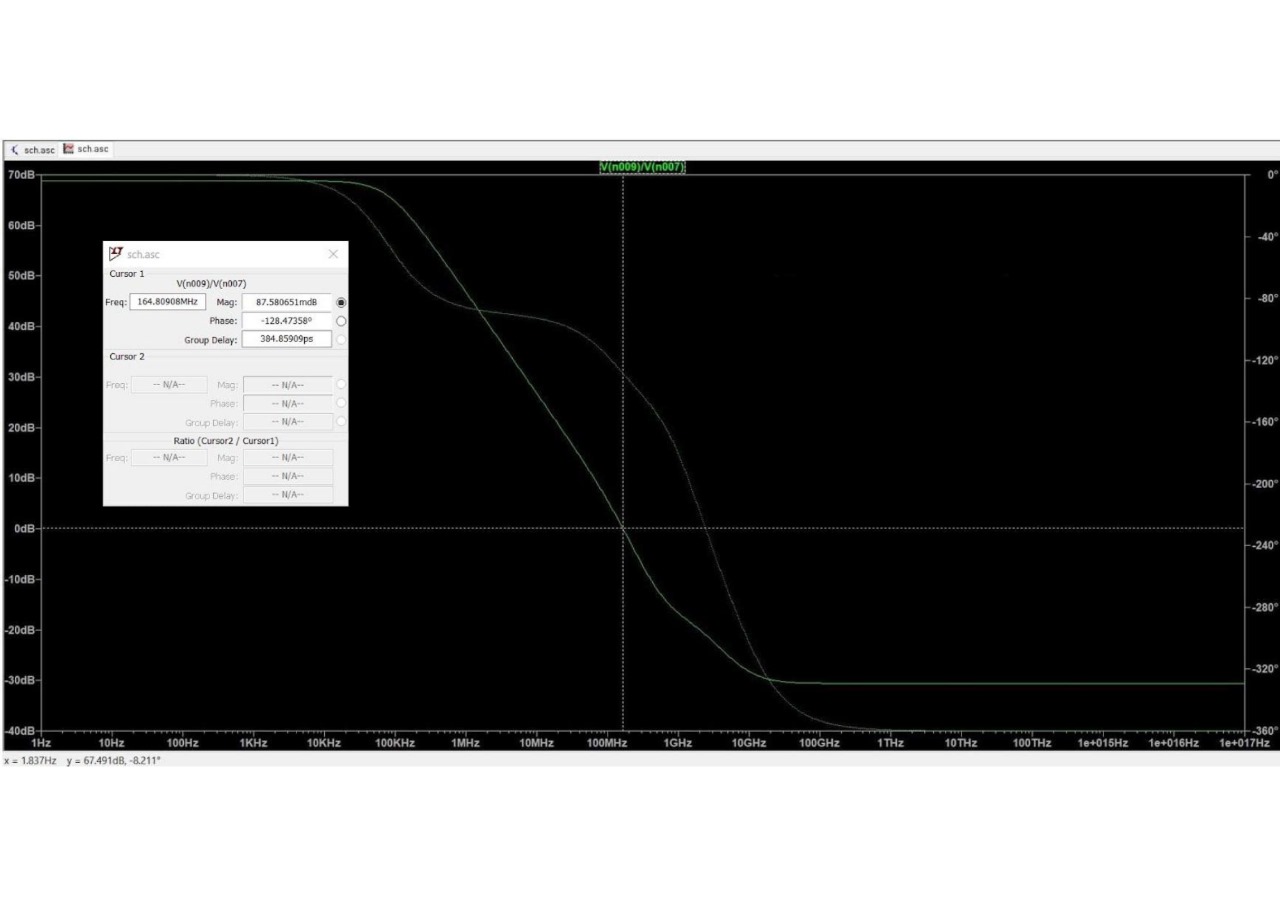


*Fig 3. O/P Swing = 2.4V > 2V*

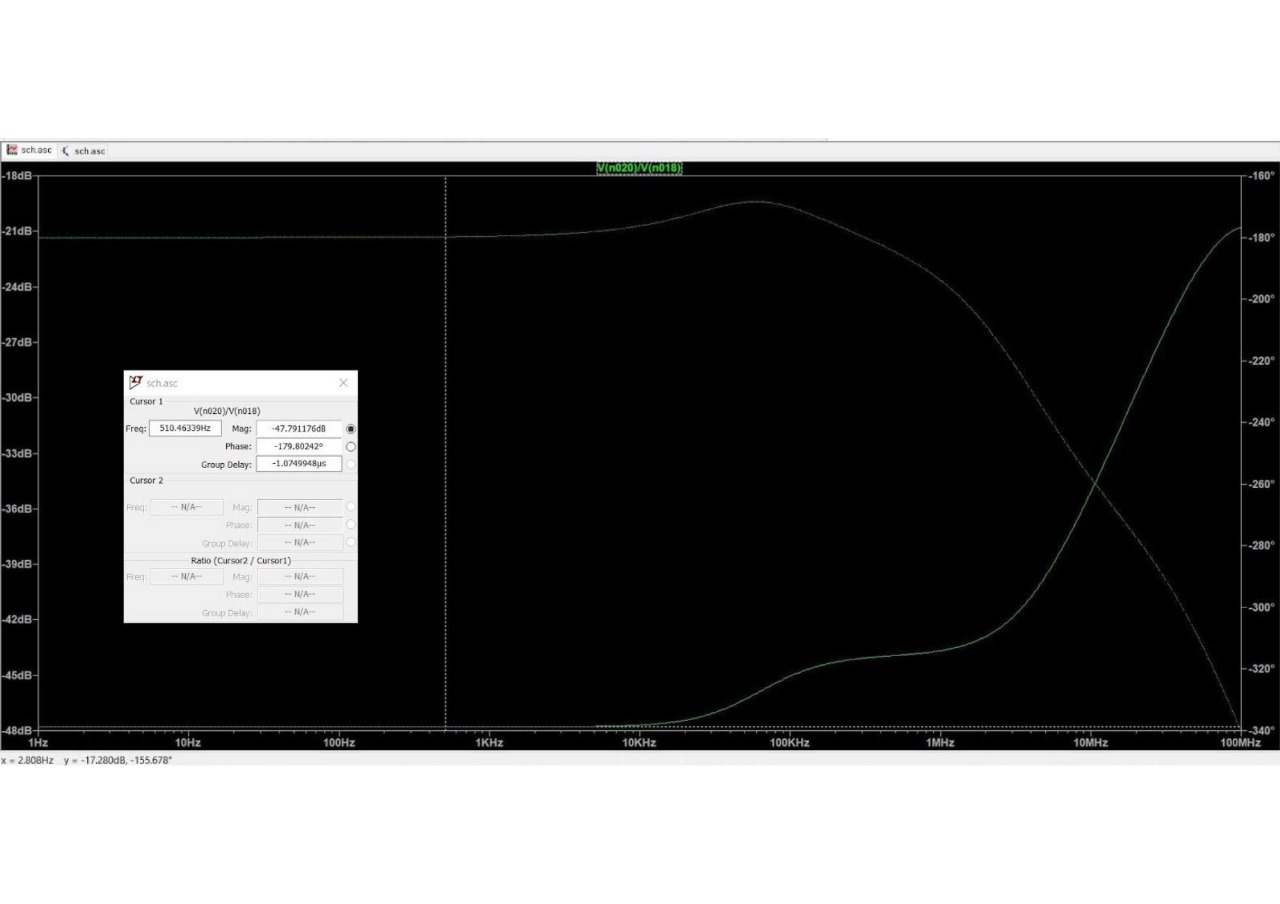
**STB Analysis -**



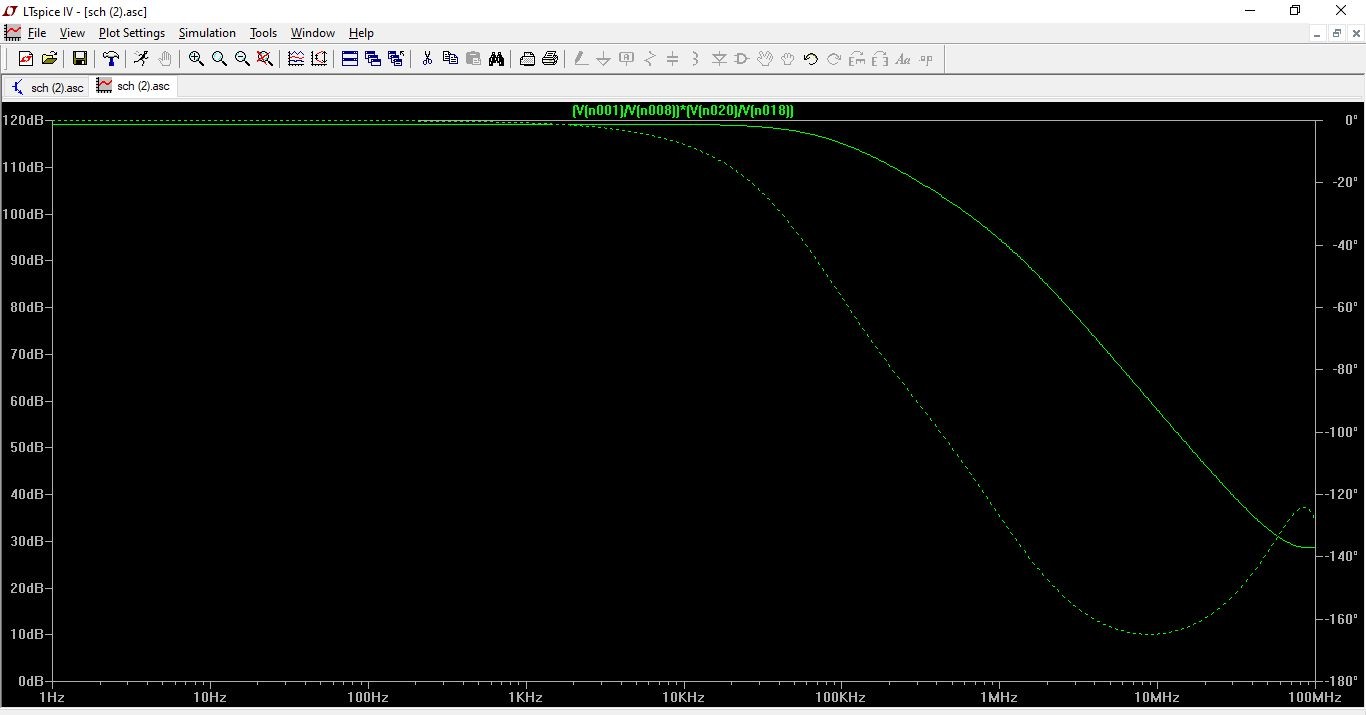
*Fig 4. Closed Loop Gain = -0.2db*

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*Fig 5. Differential Gain =70dB with phase margin = 51.2°*

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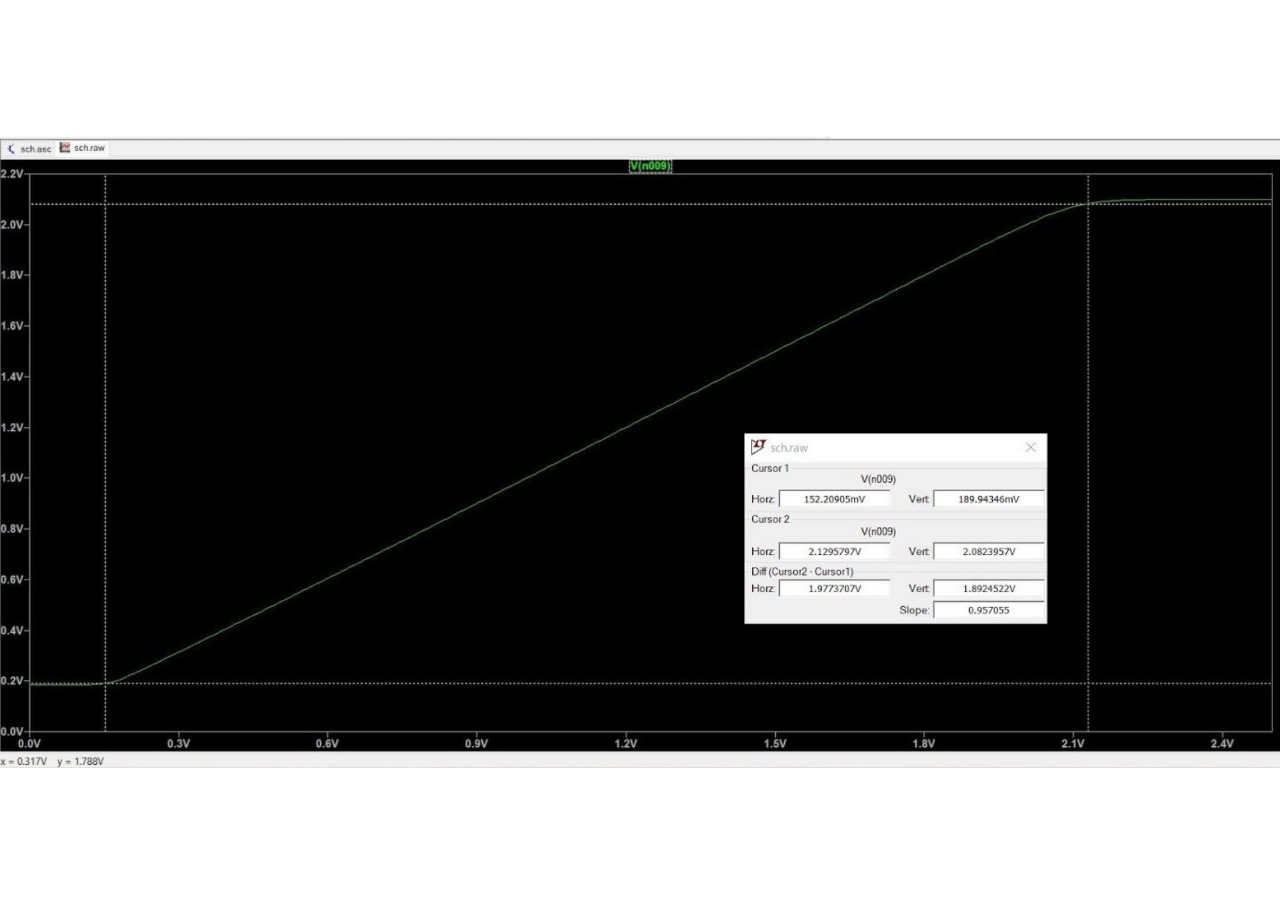
*Fig 6. Common Mode Gain = -47dB*



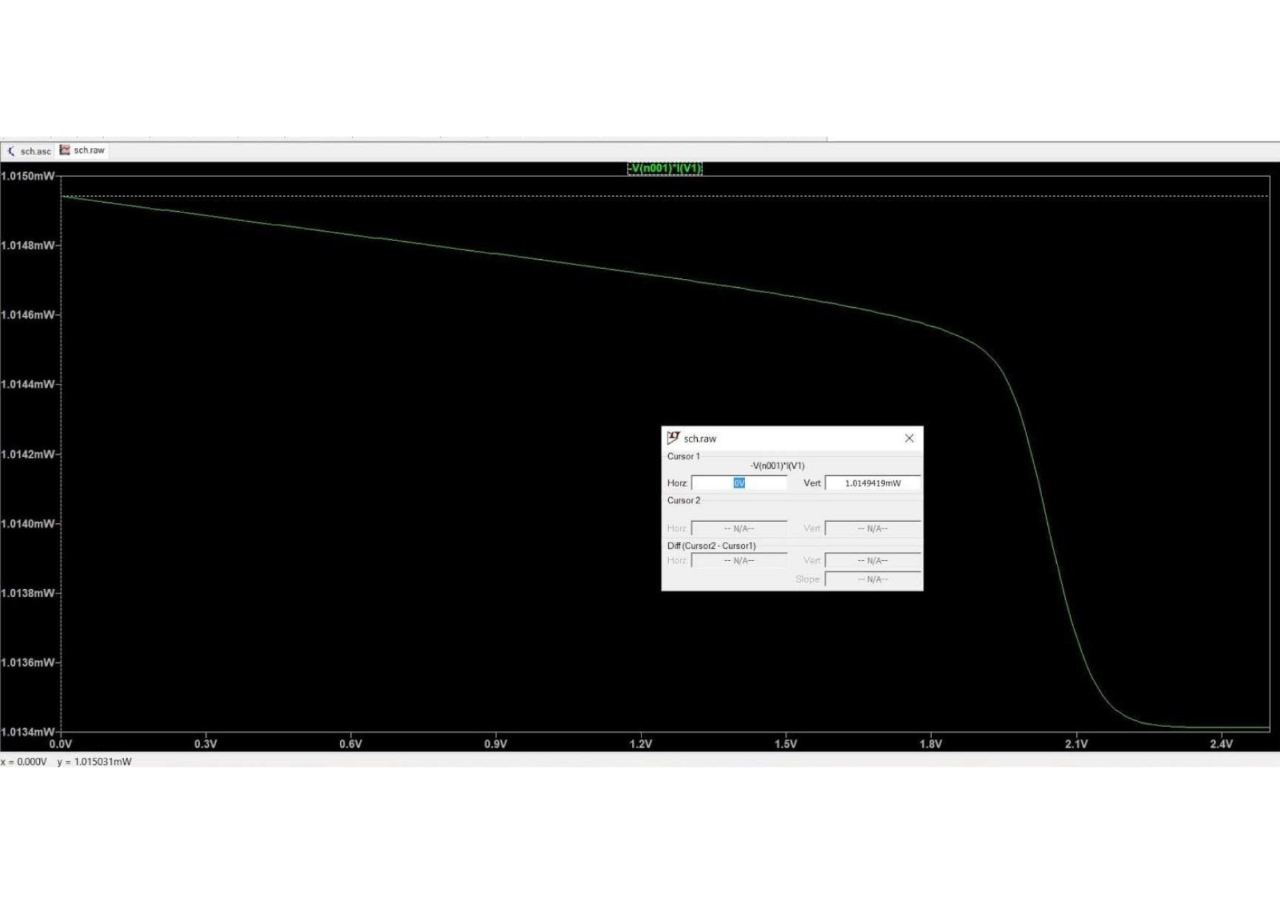
*Fig 7. PSRR Plot = 120dB*



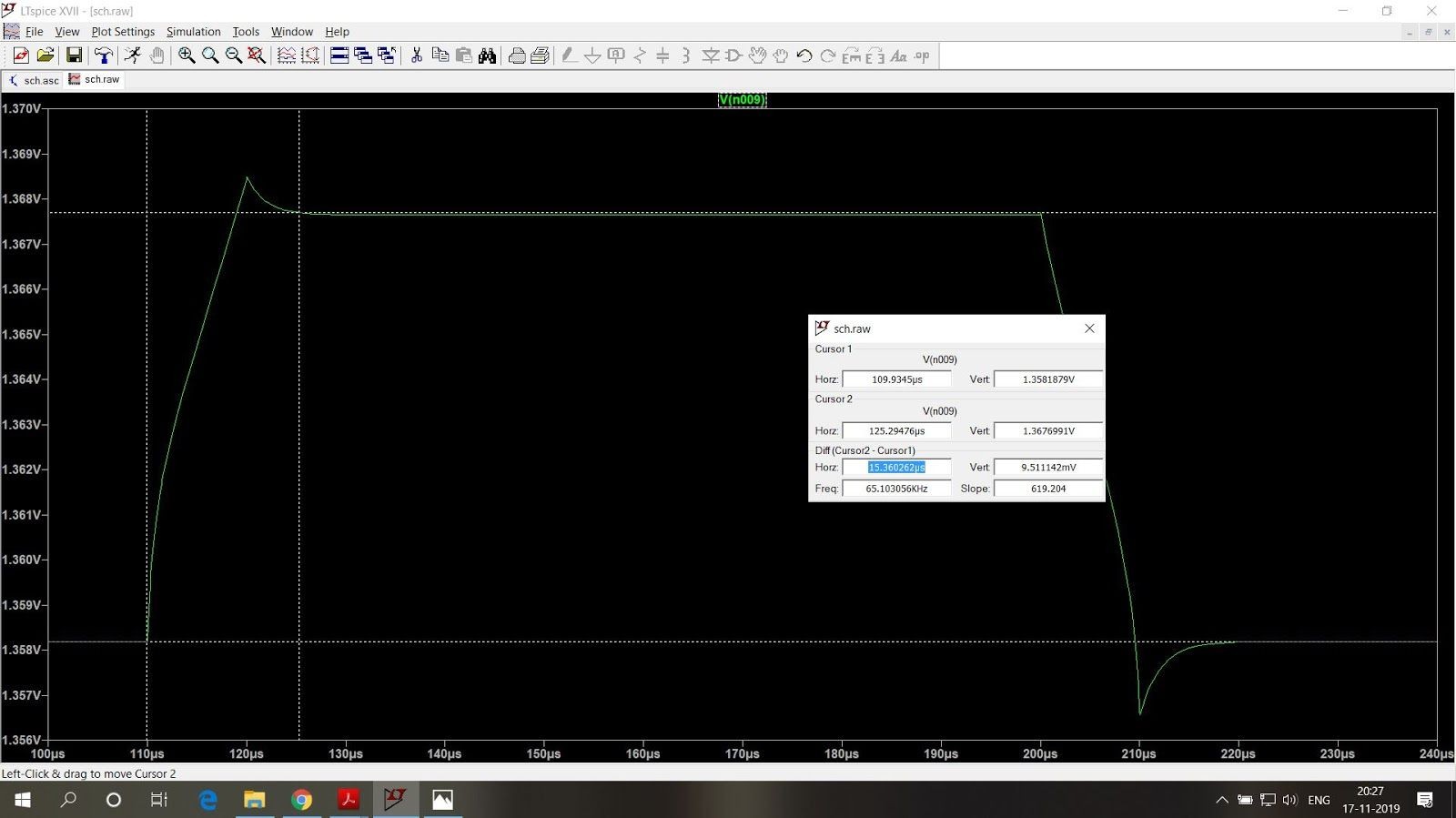
*Fig 8. Slew Rate = 1.1V/us*

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*Fig 9. Output Swing: (DC) ~2 V*

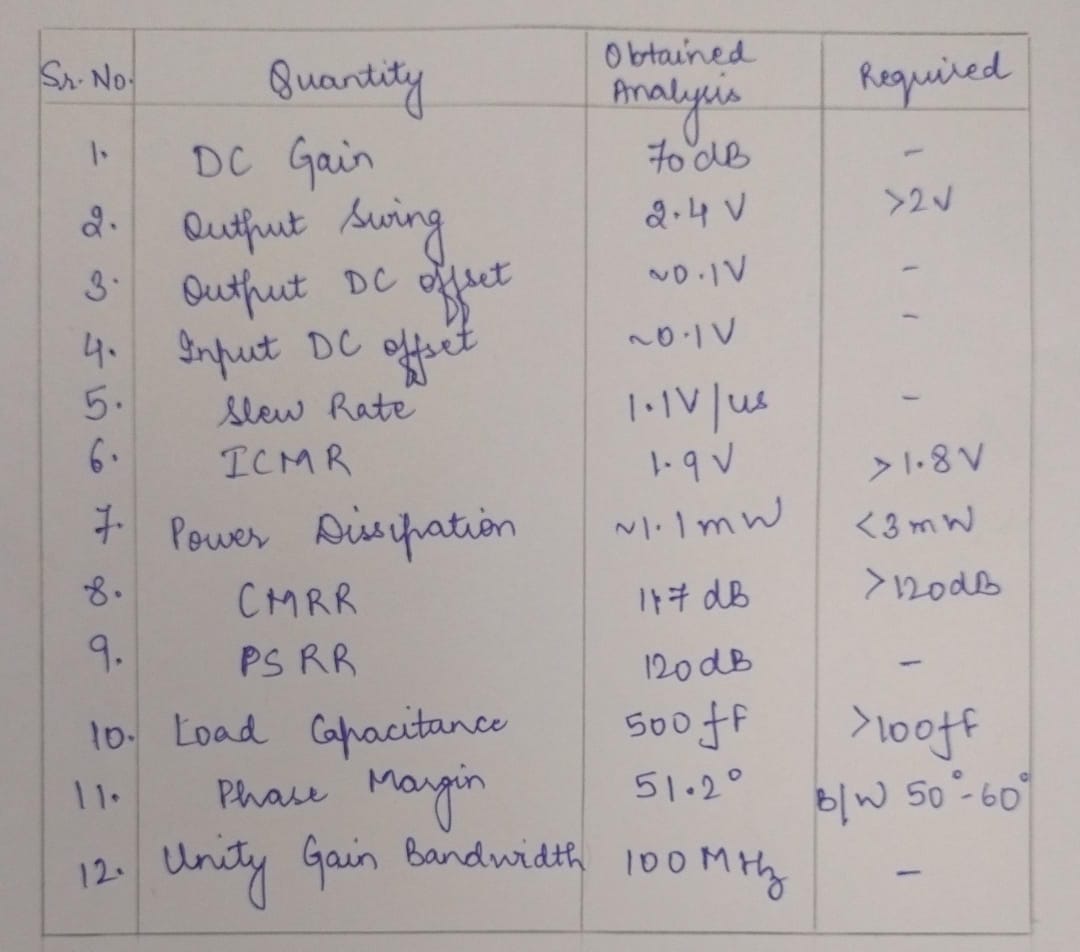


*Fig 10. Power Dissipation = 1.01mW <3mW*



*Fig 11. Settling Time = 15.3us*

**Observations and Results:**

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**Conclusion:**

The operational amplifier is designed to achieve an impressive total CMRR of 120 dB. A low current source of 50 μA was selected to ensure high gain performance. Overall, the implemented design successfully meets most of the key specifications while maintaining minimal power consumption. Additionally, it offers excellent voltage swing, high gain, and a wide input common-mode range (ICMR).

**References:**

1. Kaushik, R., & Kaur, J. (2024). Design of folded cascode op amp and its application–bandgap reference circuit. *Circuit World*, *50*(1), 9-17.
2. Nakamura, K., & Carley, L. R. (1992). An enhanced fully differential folded-cascode op amp. *IEEE Journal of Solid-State Circuits*, *27*(4), 563-568.
3. Razavi, B. (2017). *Design of analog CMOS integrated circuits* (2nd ed.) McGraw Hill.